

1. Product profile

1.1 Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance. Also includes TrenchPLUS current sensing, and diodes for ESD and temperature protection.

Product availability:

BUK7C10-75AITE in SOT427 (D²-PAK).

1.2 Features

- Q101 compliant
- ESD protection
- Integrated temperature sensor
- Integrated current sensor.

1.3 Applications

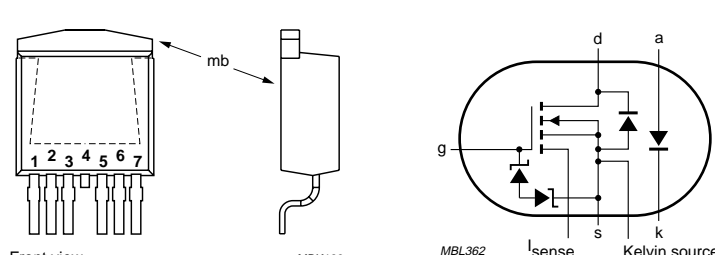
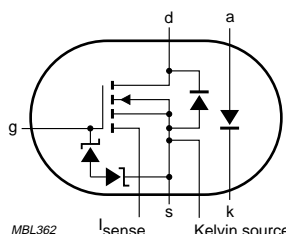
- Variable Valve Timing for engines
- Automotive and power switching
- Electrical Power Assisted Steering
- Fan control.

1.4 Quick reference data

- $V_{DS} \leq 75$ V
- $I_D \leq 114$ A
- $R_{DSon} = 8.8$ m Ω (typ)
- $V_F = 658$ mV (typ)
- $S_F = -1.54$ mV/K (typ)
- $I_D/I_{sense} = 500$ (typ).

2. Pinning information

Table 1: Pinning - SOT427 (D²-PAK) simplified outline and symbol

Pin	Description	Pin	Description	Simplified outline	Symbol
1	gate (g)	5	cathode (k)	 <p>Front view</p> <p>Side view (MBK128)</p> <p>Symbol (MBL362)</p>	 <p>g</p> <p>d</p> <p>a</p> <p>I_{sense}</p> <p>s</p> <p>k</p> <p>Kelvin source</p>
2	I_{sense}	6	Kelvin source		
3	anode (a)	7	source (s)		
4	drain (d)				
mb	mounting base; connected to drain (d)				

SOT427 (D2-PAK)

3. Limiting values

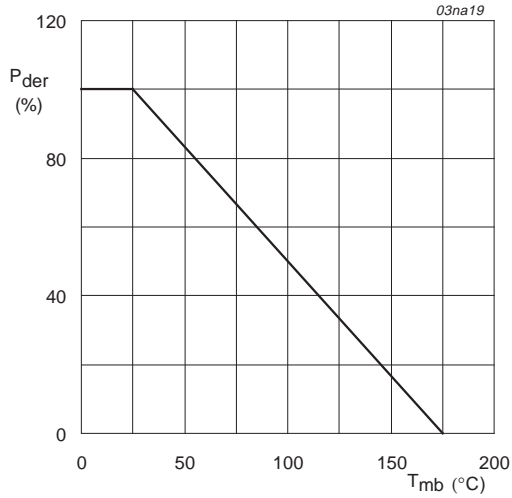
Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)		-	75	V
V_{DGS}	drain-gate voltage (DC)		-	75	V
V_{GS}	gate-source voltage (DC)		-	±20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2 and 3	[1] -	114	A
			[2] -	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 10\text{ V};$ Figure 2	[2] -	75	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	456	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	272	W
$I_{GS(CL)}$	gate-source clamping current	continuous	-	10	mA
		$t_p = 5\text{ ms}; \delta = 0.01$	-	50	mA
$V_{isol(FET-TSD)}$	FET to temperature sense diode isolation voltage		-	±100	V
T_{stg}	storage temperature		-55	+175	°C
T_j	junction temperature		-55	+175	°C
Source-drain diode					
I_{DR}	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	[1] -	114	A
			[2] -	75	A
I_{DRM}	peak reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	456	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A};$ $V_{DS} \leq 75\text{ V}; V_{GS} = 10\text{ V};$ $R_{GS} = 50\text{ }\Omega;$ starting $T_j = 25\text{ °C}$	-	739	mJ
Electrostatic discharge					
V_{esd}	electrostatic discharge voltage; pins 1,2,4,6,7	Human Body Model; $C = 100\text{ pF};$ $R = 1.5\text{ k}\Omega$	-	6	kV

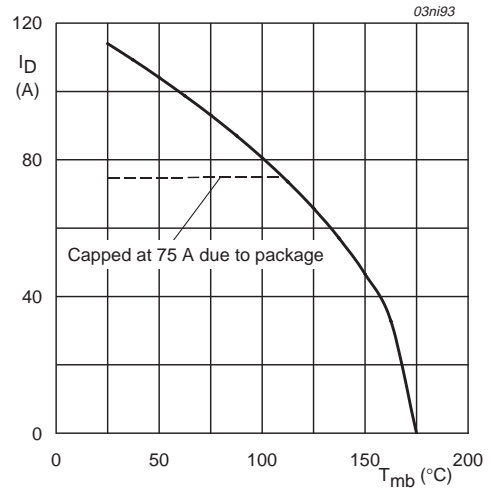
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



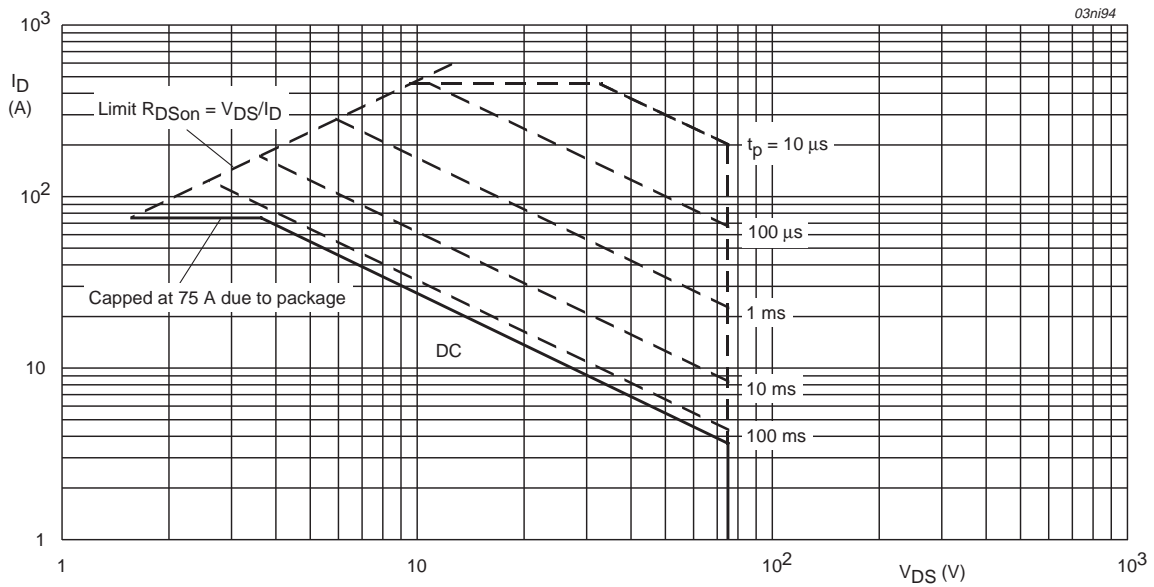
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10\text{ V}$

Fig 2. Continuous drain current as a function of mounting base temperature.



$T_{mb} = 25^{\circ}C$; I_{DM} single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	-	50	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.55	K/W

4.1 Transient thermal impedance

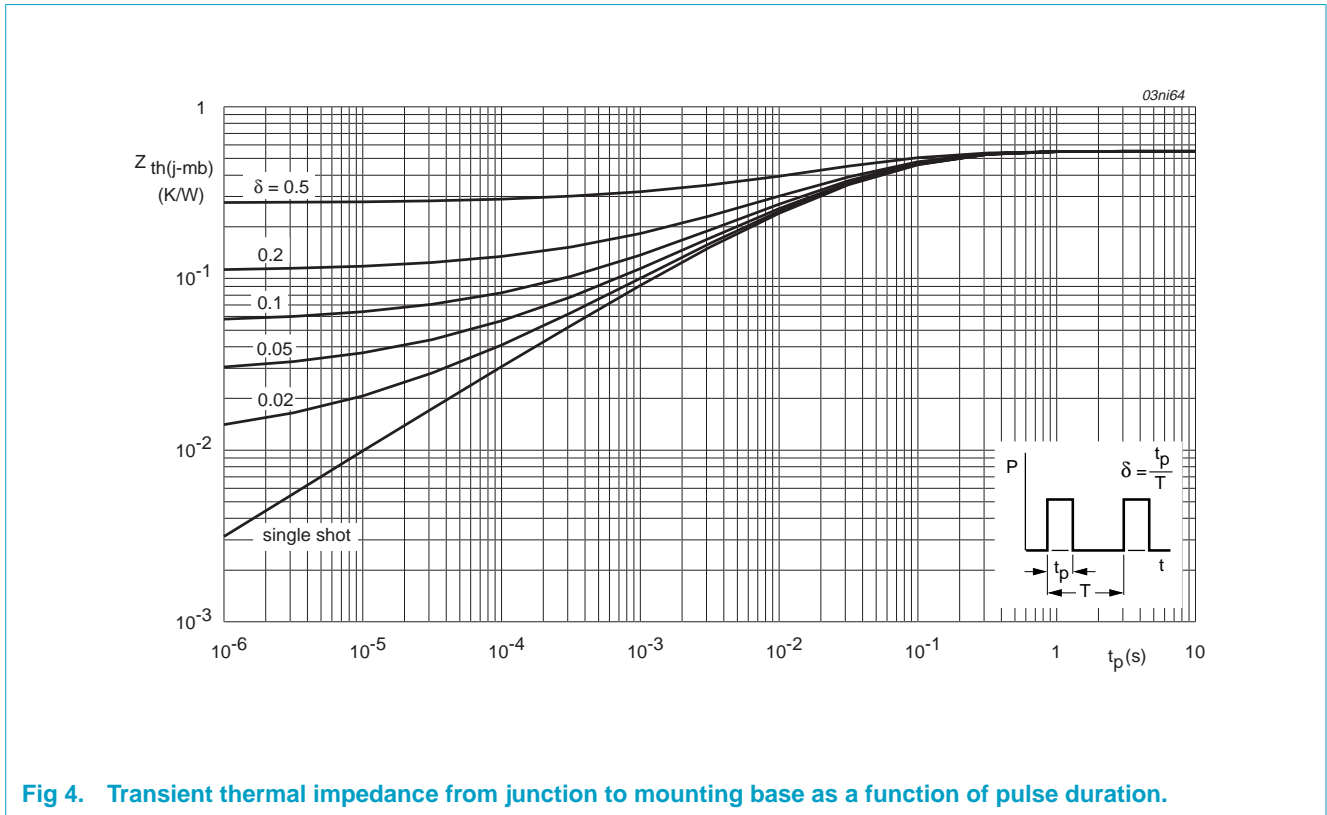


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

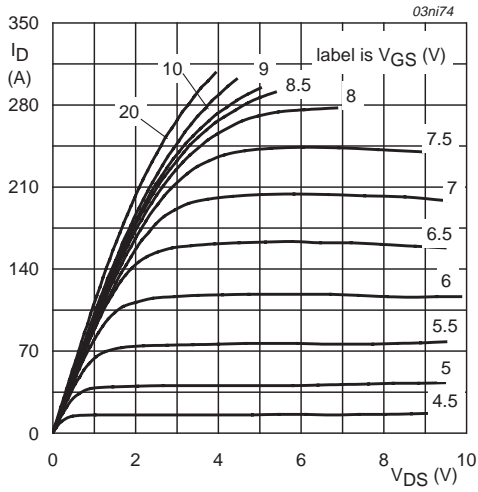
5. Characteristics

Table 4: Characteristics
 $T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25\text{ mA}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	75	-	-	V
		$T_j = -55\text{ °C}$	70	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}; V_{DS} = V_{GS};$ Figure 9				
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
I_{DSS}	drain-source leakage current	$V_{DS} = 75\text{ V}; V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.1	10	μA
		$T_j = 175\text{ °C}$	-	-	250	μA
$V_{(BR)GSS}$	gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$ $-55\text{ °C} < T_j < 175\text{ °C}$	20	22	-	V
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 10\text{ V}; V_{DS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	22	1000	nA
		$T_j = 175\text{ °C}$	-	-	10	μA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 50\text{ A};$ Figure 7 and 8				
		$T_j = 25\text{ °C}$	-	8.8	10	m Ω
		$T_j = 175\text{ °C}$	-	-	21	m Ω
V_F	forward voltage, temperature sense diode	$I_F = 250\text{ }\mu\text{A}$	648	658	668	mV
S_F	temperature coefficient temperature sense diode	$I_F = 250\text{ }\mu\text{A};$ $-55\text{ °C} < T_j < 175\text{ °C}$	-1.4	-1.54	-1.68	mV/K
V_{hys}	forward voltage hysteresis temperature sense diode	$125\text{ }\mu\text{A} < I_F < 250\text{ }\mu\text{A}$	25	32	50	mV
I_D/I_{sense}	ratio of drain current to sense current	$V_{GS} > 10\text{ V};$ $-55\text{ °C} < T_j < 175\text{ °C}$	450	500	550	
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$V_{GS} = 10\text{ V}; V_{DS} = 60\text{ V};$ $I_D = 25\text{ A};$ Figure 14	-	121	-	nC
Q_{gs}	gate-source charge		-	20	-	nC
Q_{gd}	gate-drain (Miller) charge		-	44	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V};$ $f = 1\text{ MHz};$ Figure 12	-	4700	-	pF
C_{oss}	output capacitance		-	800	-	pF
C_{rss}	reverse transfer capacitance		-	455	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30\text{ V}; R_L = 1.2\text{ }\Omega;$ $V_{GS} = 10\text{ V}; R_G = 10\text{ }\Omega$	-	35	-	nS
t_r	rise time		-	108	-	nS
$t_{d(off)}$	turn-off delay time		-	185	-	nS
t_f	fall time		-	100	-	nS

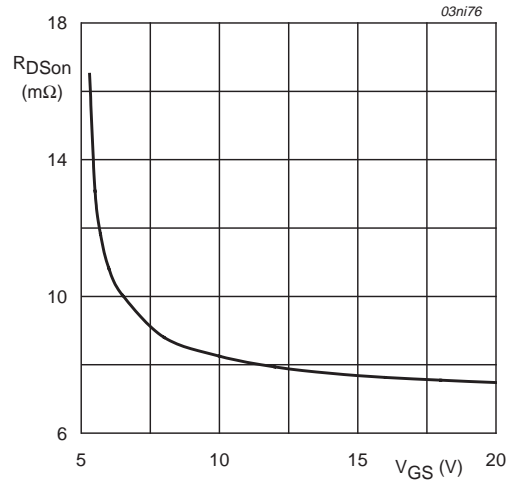
Table 4: Characteristics...continued*T_j = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L _d	internal drain inductance	measured from upper edge of drain mounting base to centre of die	-	2.5	-	nH
L _s	internal source inductance	measured from source lead to source bond pad	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 25 A; V _{GS} = 0 V; Figure 18	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs	-	75	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V	-	270	-	nC



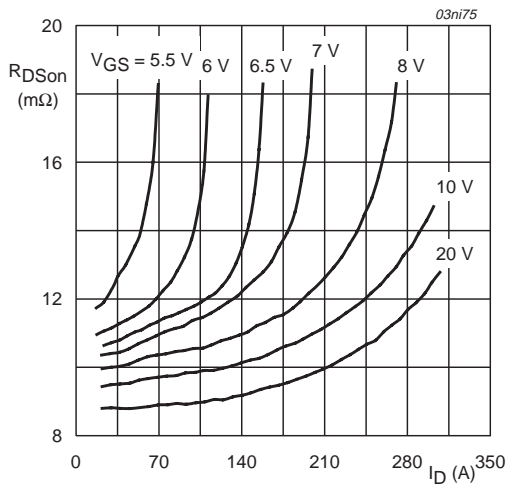
$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



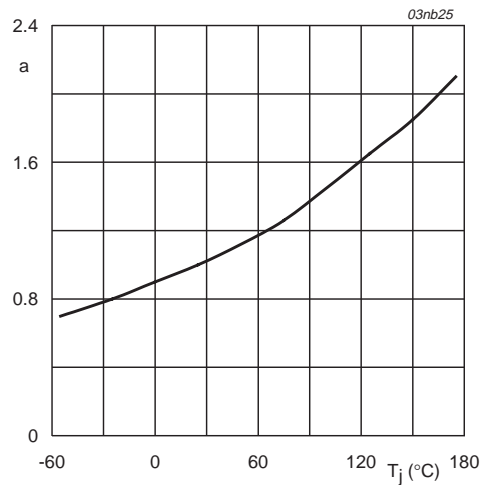
$T_j = 25\text{ }^\circ\text{C}$; $I_D = 50\text{ A}$

Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$; $t_p = 300\text{ }\mu\text{s}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



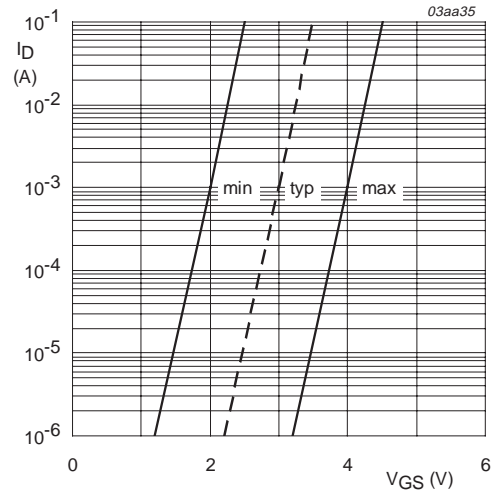
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



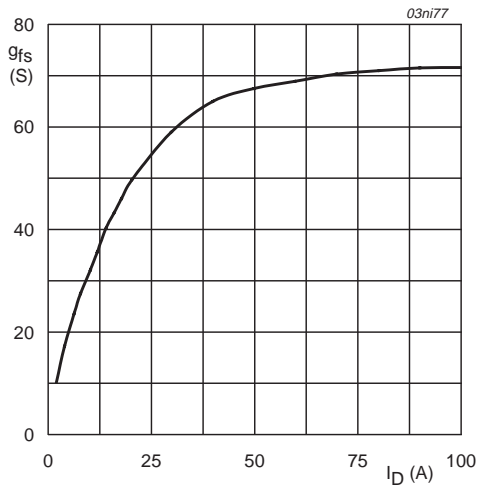
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



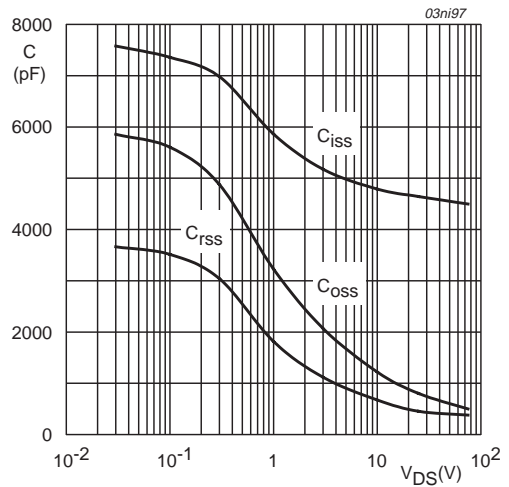
$T_j = 25 \text{ }^{\circ}C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



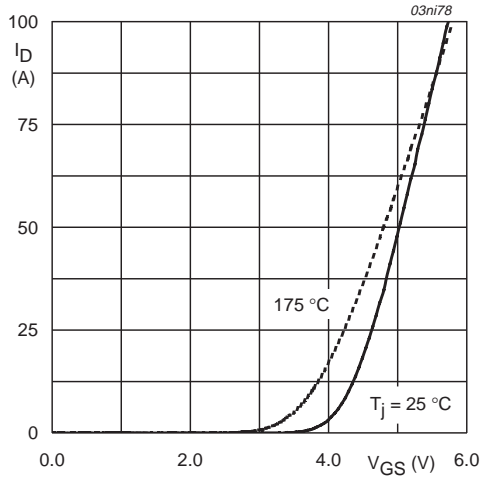
$T_j = 25 \text{ }^{\circ}C; V_{DS} = 25 \text{ V}$

Fig 11. Forward transconductance as a function of drain current; typical values.



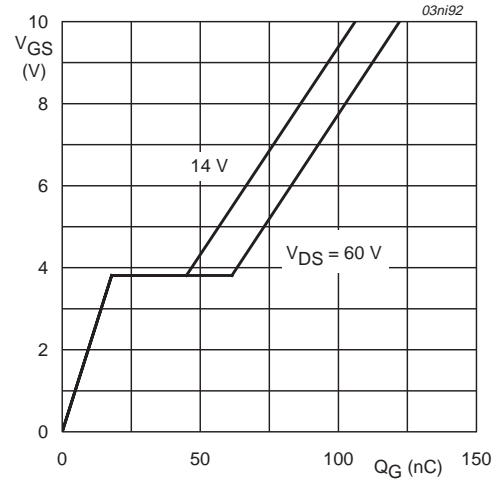
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



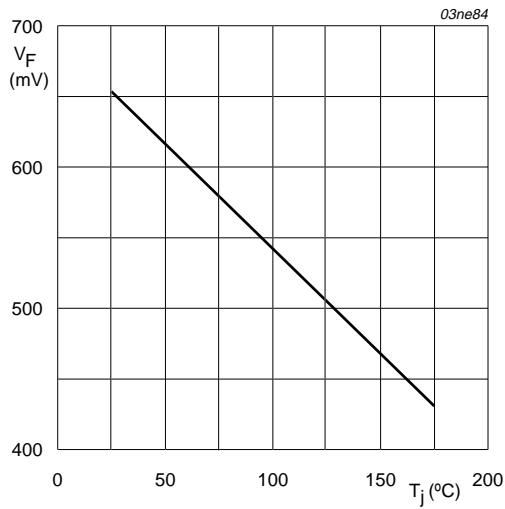
$V_{DS} = 25 \text{ V}$

Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



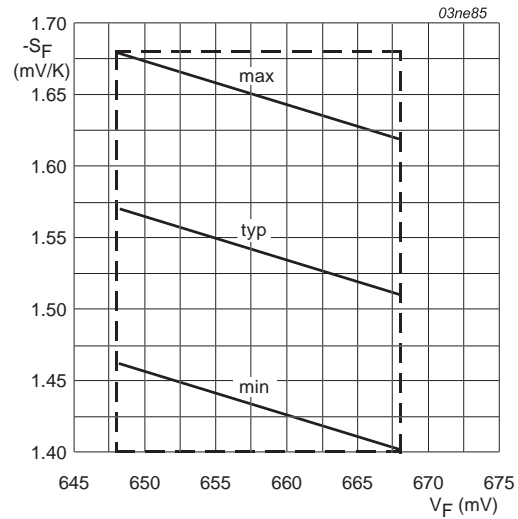
$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.



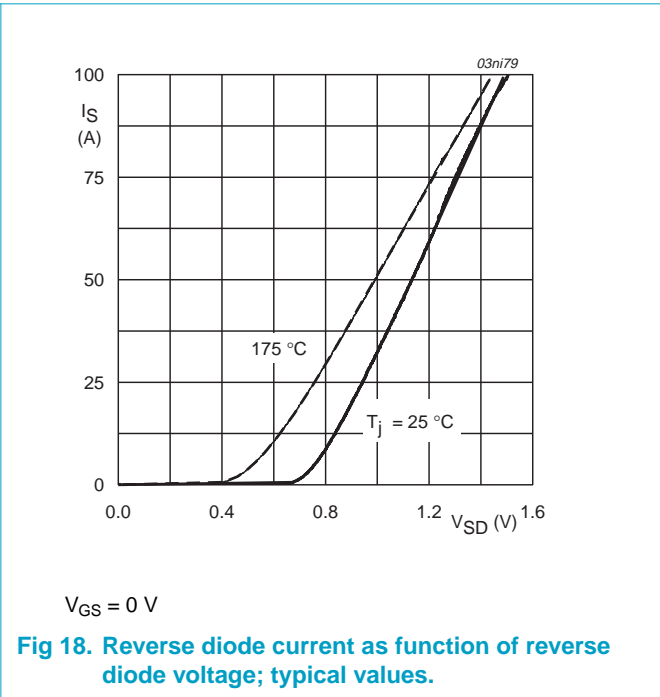
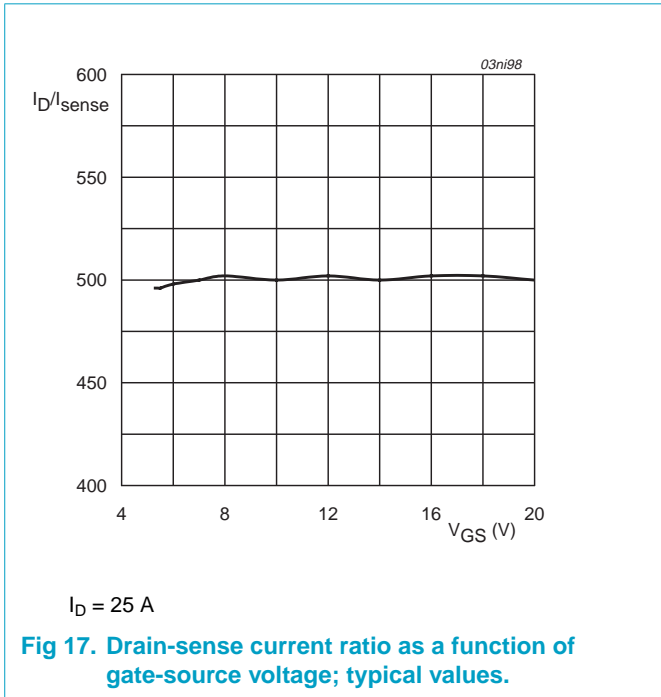
$I_F = 250 \text{ } \mu\text{A}$

Fig 15. Forward voltage of temperature sense diode as a function of junction temperature; typical values.



$V_F \text{ at } T_j = 25 \text{ }^\circ\text{C}; I_F = 250 \text{ } \mu\text{A}$

Fig 16. Temperature coefficient of temperature sense diode as a function of forward voltage; typical values.



6. Package outline

Plastic single-ended surface mounted package (Philips version of D²-PAK);
7 leads (one lead cropped)

SOT427

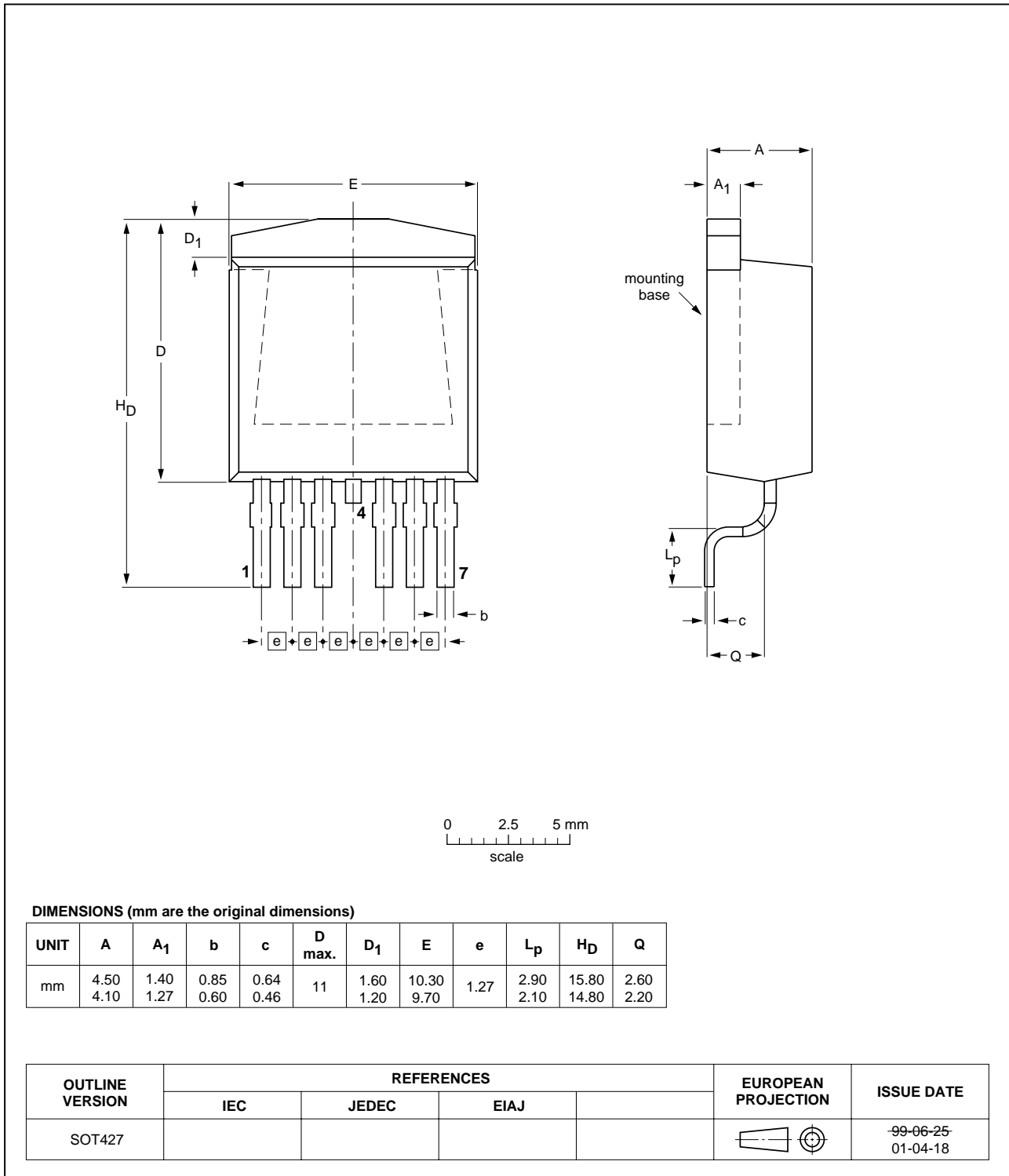
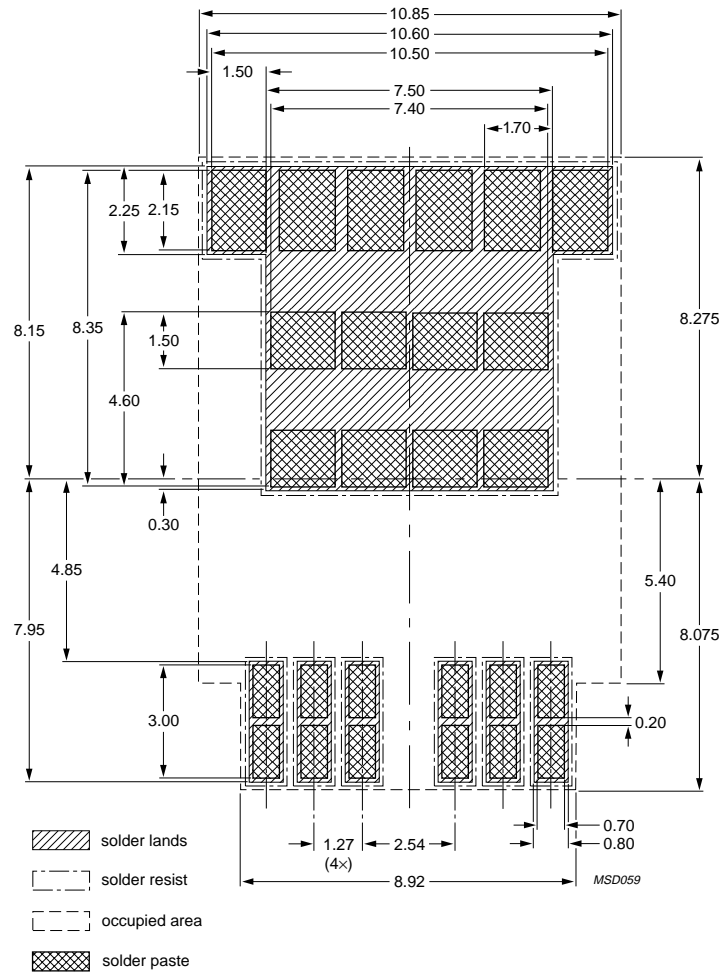


Fig 19. SOT427 (D²-PAK).

7. Soldering



Dimensions in mm.

Fig 20. Reflow soldering footprint for SOT427.

8. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20030318	-	Product data (9397 750 11048) Modification: <ul style="list-style-type: none">• Correction to Figure 3
01	20020725	-	Product data (9397 750 09881)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

10. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

11. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors

customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes in the products - including circuits, standard cells, and/or software - described or contained herein in order to improve design and/or performance. When the product is in full production (status 'Production'), relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN). Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

12. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Limiting values	2
4	Thermal characteristics	4
4.1	Transient thermal impedance	4
5	Characteristics	5
6	Package outline	11
7	Soldering	12
8	Revision history	13
9	Data sheet status	14
10	Definitions	14
11	Disclaimers	14
12	Trademarks	14

© Koninklijke Philips Electronics N.V. 2003.
Printed in The Netherlands

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 18 March 2003

Document order number: 9397 750 11048



PHILIPS

Let's make things better.